Lafia Journal of Scientific & Industrial Research (LJSIR), Vol. 3(1), 2025
p-ISSN: 3026 – 9288 e-ISSN: 3027 – 1800 pages: 90 – 97
https://lafiascijournals.org.ng/index.php/ljsir/index ⇒ Published by the Faculty of Science,
Federal University of Lafia, Nasarawa State, Nigeria

Effect of Duty Cycle Control on Performance of Sepic DC–DC Buck-Boost Converter under Resistive Load Applications

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Abstract

This paper investigates the effect of duty cycle control on the performance of the SEPIC (Single-Ended Primary Inductor Converter) DC–DC buck-boost converter, particularly when subjected to resistive load applications. The SEPIC converter, known for its ability to output a voltage either greater or lesser than the input, finds broad application in power supplies and renewable energy systems. An analysis of how the duty cycle influences key performance metrics, such as output voltage, currents and voltage ripple is presented. Simulation result demonstrate that careful modulation of the duty cycle enables optimization of converter performance, offering valuable insights into how these converters can be tuned to enhance efficiency inresistive load scenarios. The results obtained reveal that the Sepic dc dc converter is capable of delivering a maximum output power approximately 1857 W at dutycycle of 80% with 20 kHz switching frequency. Also, at the same switching frequency, 20% duty cycle, a minimum output power of approximately 5.34 W was obtained. These insights are valuable for power electronics engineers seeking to optimize SEPIC converters for domestic load applications.

Keywords: Sepic converter, duty cycle, resistive load, voltage control

Article History
Submitted
January 10, 2025
Revised
March 22, 2025
First Published Online
March 26, 2025

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doi.org/10.62050/ljsir2025.v3n1.488

Introduction

DC–DC converters are fundamental components in power electronics, enabling voltage regulation across a variety of applications, from renewable energy systems to battery-operated devices. The SEPIC converter [1, 2], a versatile topology, is capable of operating in buck [3-11], boost [12-16], and buck-boost [17] modes by varying its duty cycle. This feature is especially useful for applications requiring stable output voltage despite fluctuating input voltages. It is very vital to use alternative energy sources to supply the demand along with the traditional sources, in as much as the technological development and worldwide consumption of electricity continues to grow [18].

The duty cycle, defined as the proportion of the switching period where the switch is "on," is critical in determining the output characteristics of the SEPIC converter. By adjusting the duty cycle, the SEPIC converter can efficiently handle changes in input voltage and load conditions, thereby improving performance metrics like output stability, conversion efficiency, and voltage ripple [19, 20]. Duty cycle control offers a method to adaptively manage power conversion under different resistive load conditions, ensuring robust operation across a range of applications. To ensure that the power supply and other components are not being over-loaded, the SEPIC runs in continuous conduction mode all the time. This technique may be used to create a switching pulse or duty cycle for the SEPIC's MOSFET switch.

The main contribution of this paper is applying variable duty cycle to control the SEPIC converter output voltage at different switching frequency. The use of DC voltage value to compare a saw-tooth carrier signal are required to obtained any value of duty cycle for the control. This will aid researchers in component or parameter selection for the Sepic converter design.

Materials and Methods

This work is based on software-based simulation and the approach followed Sepic converter mathematical analysis and design, and pulse width modulation design as depicted in Fig. 4.

Design specifications of SEPIC converter

The Sepic buck-boost dc to dc converter has the same principle of operation as Cuk's buckboost converter but has inductors L_{m1}, L_{m2} and C_m arranged in a manner that gives positive converter output voltage. The circuit configuration is as depicted in Fig. 1.

For the interval $0 \leq t \leq DT$ in a cycle, the switch S_m is turned on as depicted in Fig. 1, thus causing diode D_m to be reverse biased. The sum of the inductor currents ($i_{Lm1} + i_{Lm2}$), therefore, flows through the switch Sm. Mathematically,

$$V_{Lm1} = V_{in} \quad (1)$$

$$V_{Lm2} = -V_{cm} \quad (2)$$

The resultant changes in inductor currents ($\Delta i_{Lm1} and\ \Delta i_{Lm2}$) in the interval therefore become

$$i_{Lm1max} - i_{Lm1min} = \Delta i_{Lm1} = \frac{V_{in}D}{fL_{m1}} \quad (3)$$

$$i_{Lm2max} - i_{Lm2min} = \Delta i_{Lm2} = \frac{V_{cm}D}{fL_{m2}} \quad (4)$$

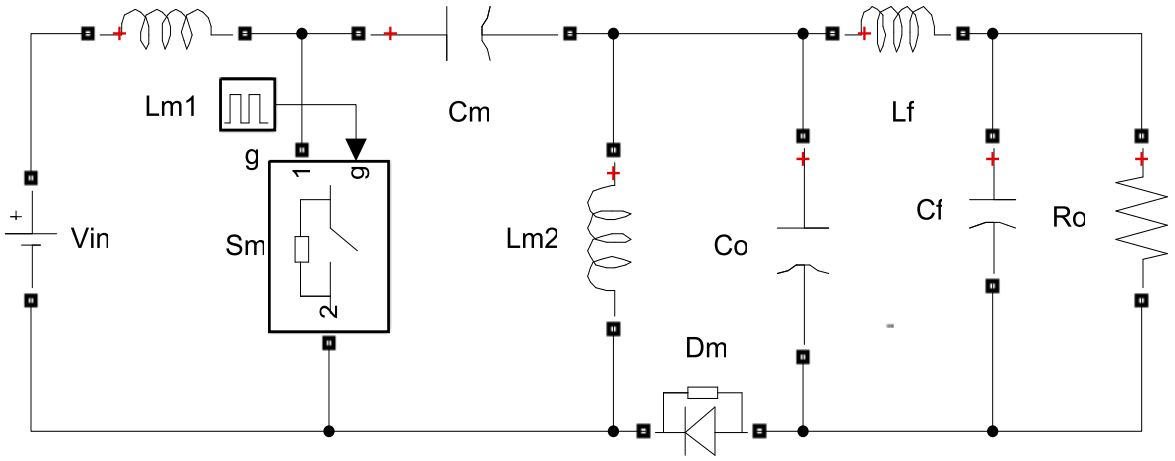

Figure 1: The Sepic buck-boost dc to dc converter circuit topology

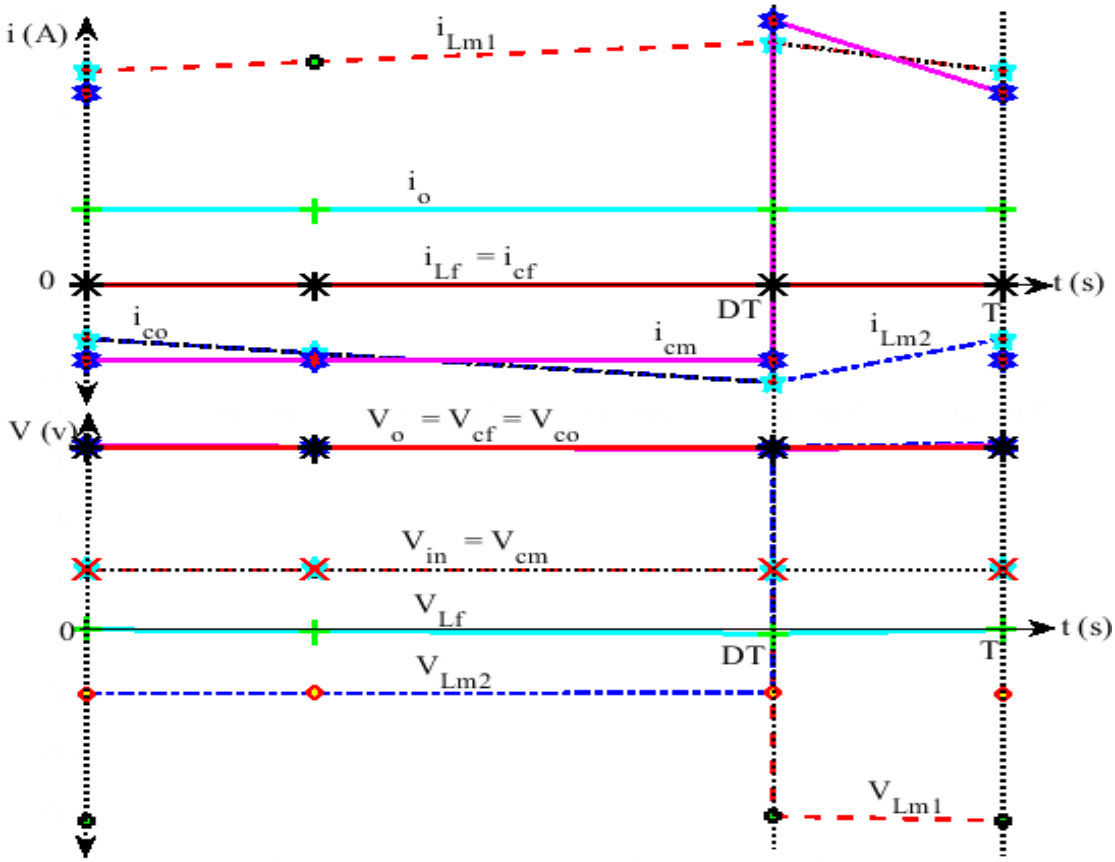

Figure 2: Continuous diode current operation of Sepic converter

For the remaining interval DT ≤ t ≤ T in a cycle of period T, as indicated in Fig. 2, the switch Sm in Fig. 1 is turned off and the sum of ((i_{Lm1} + i_{Lm2}) of the inductor currents flow through the diode Dm. This makes the inductor voltages to become

$$V_{Lm1} = -V_o \quad (5)$$

$$V_{Lm2} = V_{in} - V_{cm} - V_o \quad (6)$$

The resultant changes in inductor currents ($\Delta i_{Lm1} and\ \Delta i_{Lm2}$) in the interval therefore become

$$i_{Lm1max} - i_{Lm1min} = \Delta i_{Lm1} = \frac{V_o(1-D)}{fL_{m1}} \quad (7)$$

$$i_{Lm2max} - i_{Lm2min} = \Delta i_{Lm2} = \frac{-(V_{in} - V_{cm} - V_o)(1-D)}{fL_{m2}} \quad (8)$$

Comparing equations (3), (4) and (7), (8) respectively, give the result

$$\frac{V_{cm}}{V_{in}} = 1 \quad (9)$$

$$\frac{V_o}{V_{cm}} = \frac{D}{1-D} \quad (10)$$

That is,

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \quad (11)$$

Assuming a lossless system we have, P_{in} =P_{out} therefore, the current gain can be expressed as

$$\frac{I_{in}}{I_o} = \frac{D}{1-D} \quad (12)$$

The minimum and maximum instantaneous current i_{Lm1} in L_{m1} inductances are given as

$$i_{Lm1min} = I_{in} - \frac{\Delta i_{Lm1}}{2} \quad (13)$$

$$i_{Lm1max} = I_{in} + \frac{\Delta i_{Lm1}}{2} \quad (14)$$

Where the peak to peak ripple current Δi_{Lm1}through the inductor L_{m1} is given by

$$\Delta i_{Lm1} = \frac{V_{in}D}{fL_{m1}} = \frac{V_o(1-D)}{fL_{m1}} \quad (15)$$

Similarly, the minimum and maximum instantaneous current i_{Lm2} in L_{m2} inductances are given as

$$i_{Lm2min} = I_o - \frac{\Delta i_{Lm2}}{2} \quad (16)$$

$$i_{Lm2max} = I_o + \frac{\Delta i_{Lm2}}{2} \quad (17)$$

Where the peak to peak ripple current Δi_{Lm2}through the inductor L_{m1} is given by

$$\Delta i_{Lm2} = \frac{V_{in}D}{fL_{m2}} = \frac{V_o(1-D)}{fL_{m2}} \quad (18)$$

By considering the currents i_{cm} and i_{co} in Fig. 2 through capacitance C_m and C_o respectively, the capacitor peak to peak ripple voltages ΔV_{cm} and ΔV_{co} are respectively obtained as

$$\Delta V_{cm} = \frac{I_o D}{fC_m} \quad (19)$$

$$\Delta V_{co} = \frac{I_o D}{fC_o} \quad (20)$$

Equations (15), (18), (19) and (20) can be used to design the Sepic circuit elements. Fig. 3 displays the plots of voltage and current gains relationship between the duty cycle.

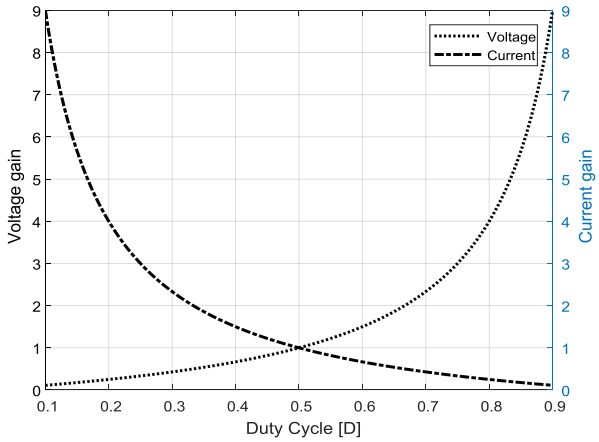

Figure 3: Voltage and current gains plot against duty cycle

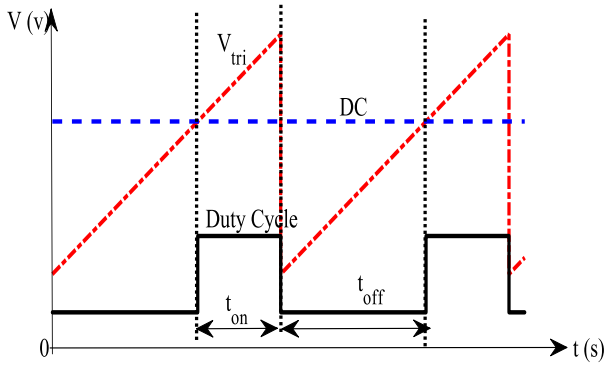

Figure 4: Pulse width modulation generation

Duty cycle control

The duty cycle (D) represents the fraction of time the signal is high (t_{on}) during one period (T) as depicted in Fig. 4.

$$D = \frac{t_{on}}{T} \quad (21)$$

Where t_{on} is when the time the signal is high; T is the total period of the signal (T= t_{on} + t_{off})

Results and Discussion

The simulations were done using the software MATLAB R2017b. All the components were assumed to be ideal. The results are discussed based on dynamic and steady state conditions. Two parameters duty cycle and switching frequency are varied to ascertain the behaviour of the circuit. Table 2 shows the system parameter specifications.

Dynamic analysis

The duty cycle is varied from 0.2 to 0.8 in step of 0.2 at different switching frequency as depicted in Fig. 5. The supply voltage with the respective duty cycle with output voltages is displayed. At 5 kHz switching frequency, Fig. 5(a) is obtained with initial overshoot voltages and attain stability before 0.05 sec. Fig. 5(b) is obtained at a switching frequency of 10 kHz while Fig. 5(c-d) are obtained at 15 kHz and 20 kHz, respectively.

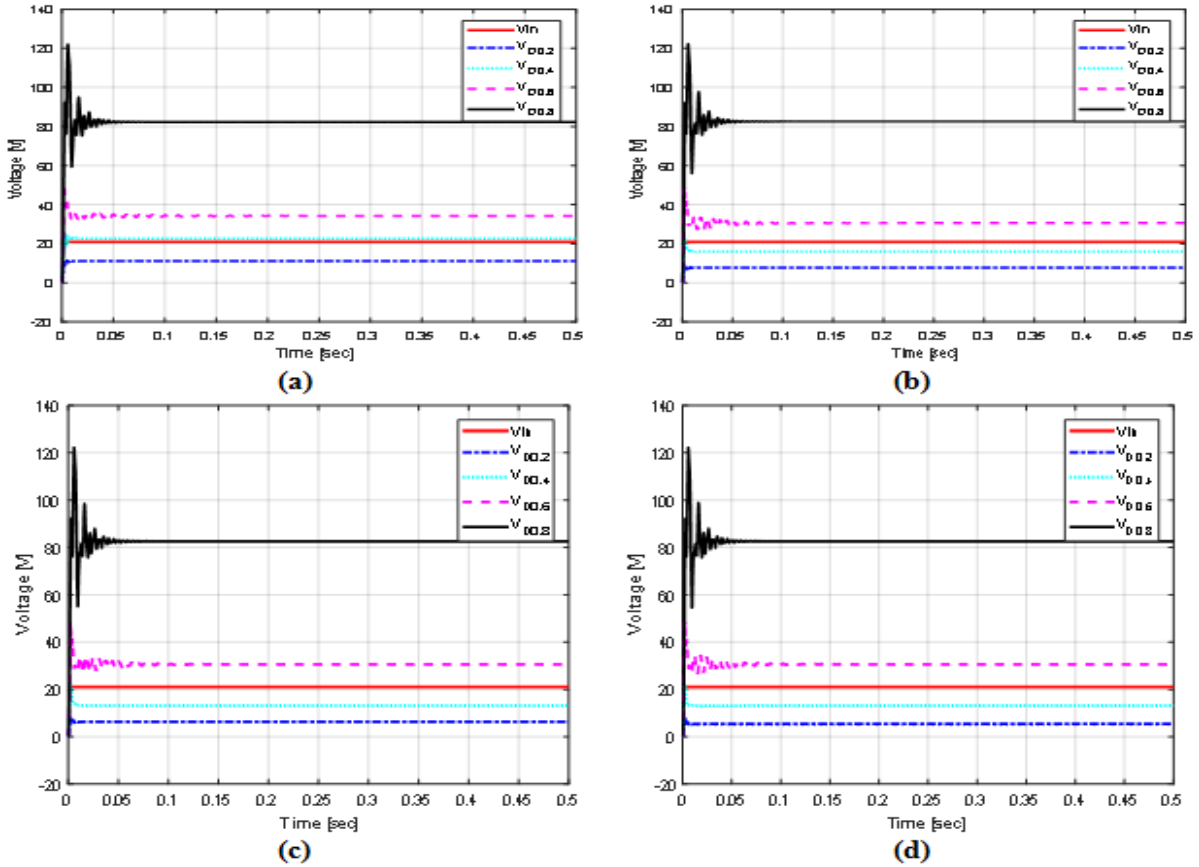

Figure 5: Output voltage waveforms (a) plots at 5 kHz switching frequency, (b) plots at 10 kHz switching frequency, (c) plots at 15 kHz switching frequency and (d) plots at 20 kHz switching frequency

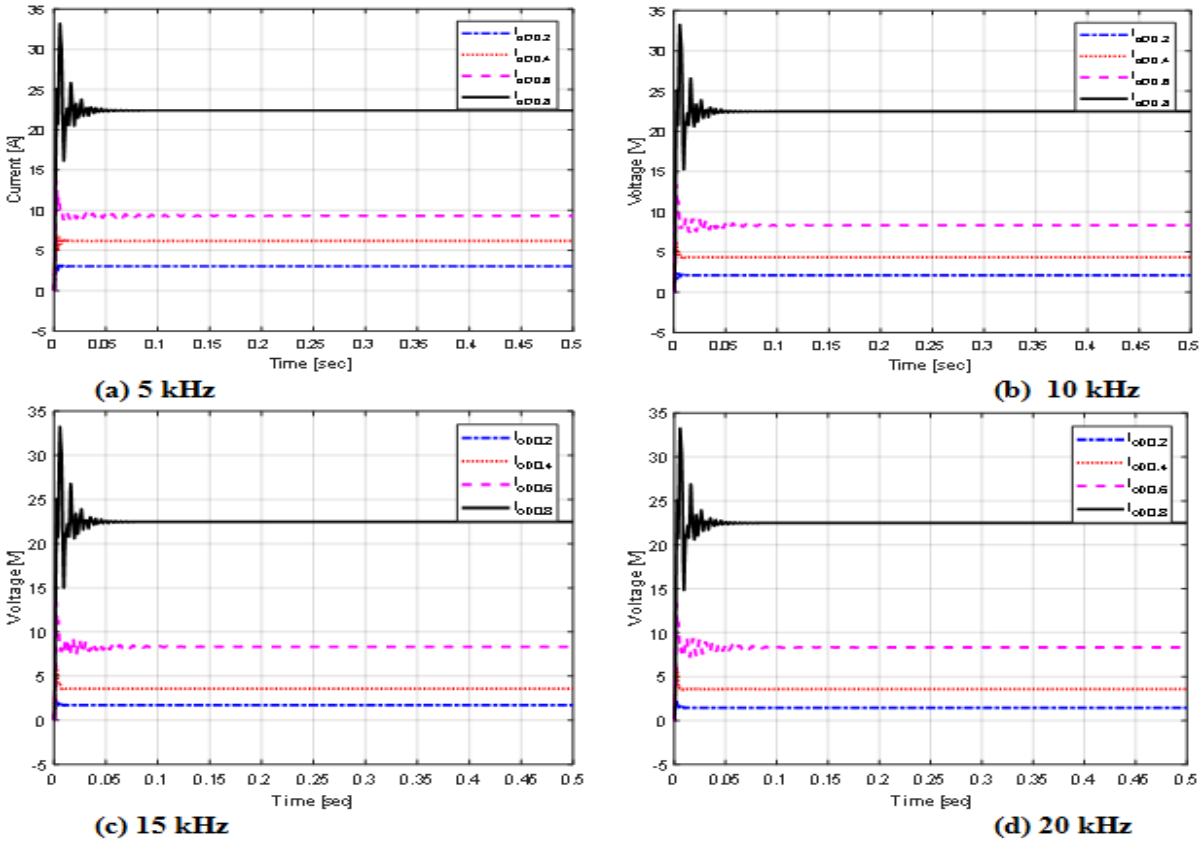

Figure 6: Output currents waveform (a) plots at 5 kHz switching frequency, (b) plots at 10 kHz switching frequency, (c) plots at 15 kHz switching frequency and (d) plots at 20 kHz switching frequency

The duty cycle is varied from 0.2 to 0.8 in step of 0.2 at different switching frequency as depicted in Fig. 6. The respective duty cycle with output currents are displayed. At 5 kHz switching frequency, Fig. 6(a) is obtained with initial overshoot voltages and attain stability before 0.05 sec. Fig. 6(b) is obtained at a switching frequency of 10 kHz while Fig. 6(c-d) are obtained at 15 kHz and 20 kHz, respectively.

The output power rating of the converter varies with respect to the value of the duty cycle as depicted in Fig. 7. At 0.8 duty ratio, the output power showed a very high transient behaviour with a high-power rating achieved at the steady state.

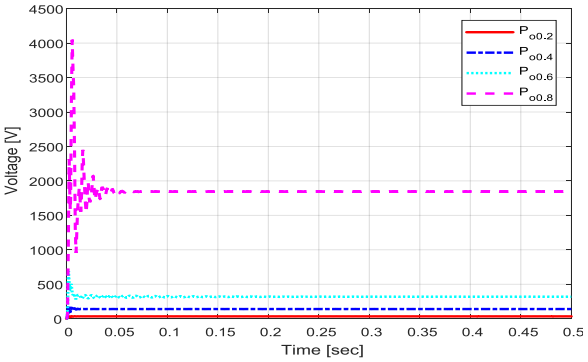

Figure 7: Output power waveforms at different duty cycle with 20 kHz switching frequency

Steady state analysis

The results generated in this subsection are taken between a time intervals as depicted in Fig. 8. Also, the duty cycle is varied from 0.2 to 0.8 in step of 0.2 at different switching frequency. The supply voltage with the respective duty cycle output voltages are displayed. At 5 kHz switching frequency, Fig. 8(a) is obtained after the system has attained stability with output voltages of different magnitude at a variable duty cycle displayed. Fig. 8(b) is obtained at a switching frequency of 10 kHz with a stable output voltage at variable duty cycle. Fig. 8(c-d) are obtained at 15 kHz and 20 kHz respectively and also, the output voltages at different duty cycle are displayed.

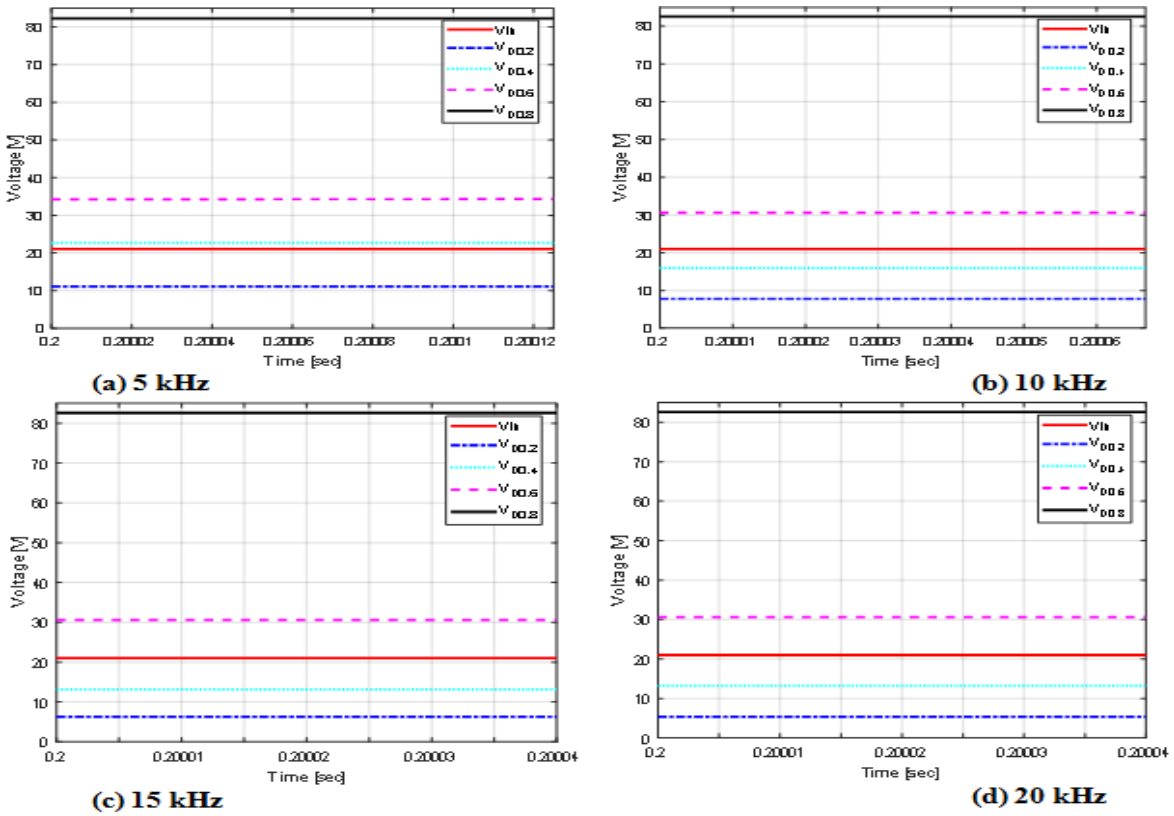

Figure 8: Output voltage waveforms after attaining stability (a) plots at 5 kHz switching frequency, (b) plots at 10 kHz switching frequency, (c) plots at 15 kHz switching frequency and (d) plots at 20 kHz switching frequency

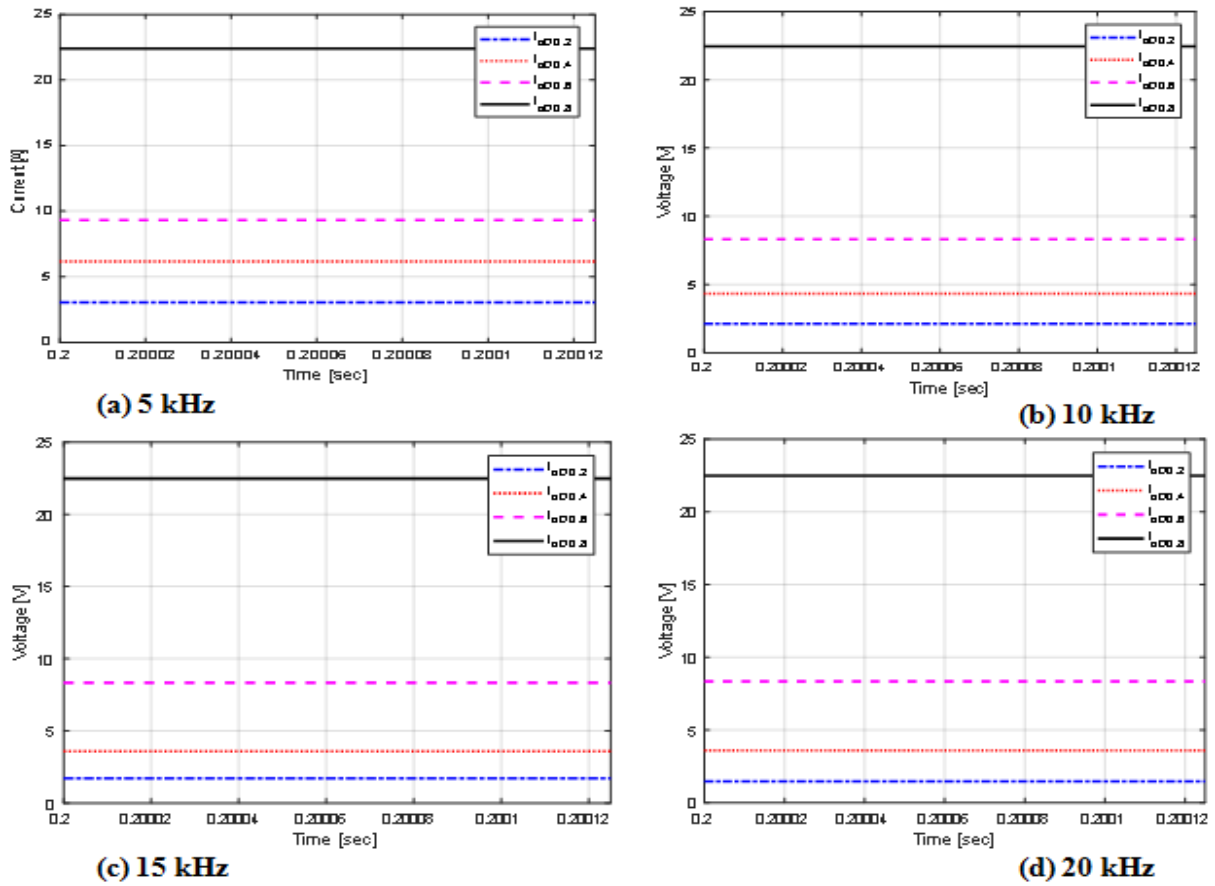

Figure 9: Output current waveforms after attaining stability (a) plots at 5 kHz switching frequency, (b) plots at 10 kHz switching frequency, (c) plots at 15 kHz switching frequency and (d) plots at 20 kHz switching frequency

The results generated in this subsection are taken between a time intervals as depicted in Fig. 9. Also, the duty cycle is varied from 0.2 to 0.8 in step of 0.2 at different switching frequency with their output currents displayed. At 5 kHz switching frequency, Fig. 9(a) is obtained after the system has attained stability with output currents of different magnitude at a variable duty cycles displayed. Fig. 9(b) is obtained at a switching frequency of 10 kHz with a stable output current at variable duty cycle. Fig. 9(c-d) is obtained at 15 kHz and 20 kHz respectively and also, the output currents at different duty cycle are displayed.

The output power rating of the converter as obtained in Fig. 10 which varies with respect to the value of the duty cycle is displayed. At switching frequency of 20 kHz, with 0.2 duty ratio, an output power of 7.862 W was obtained, at duty cycle of 0.4 an output power rating of 47.21 W was obtained, at duty ratio of 0.6 and an output power rating of 255.1 W was obtained. Also, when the duty cycle becomes 0.8, an output power rating of 1.857 kW was achieved. Table 1 shows the outputs voltage and currents based on the theoretical formular and computer aided results. The specification parameters used for the circuit calculations and simulations are depicted in Table 2.

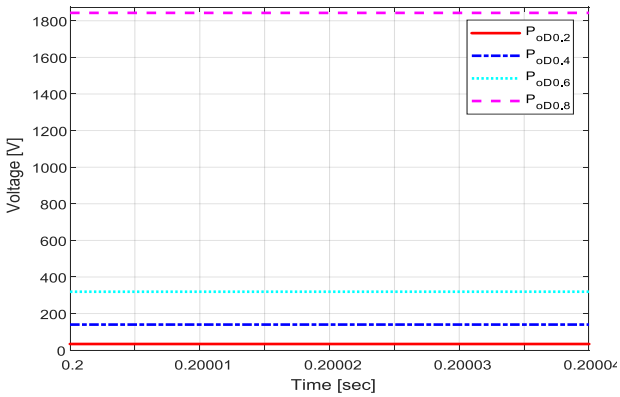

Figure 10: Output power waveforms at different duty cycle with 20 kHz switching frequency at steady state

Table 1: Summary of calculated and simulated outputs voltage and current

Duty Cycle	Calculated		Simulated (5 kHz)		Simulated (10 kHz)		Simulated (15 kHz)		Simulated (20 kHz)	
	V_o(V)	I_o(A)	V_o(V)	I_o(A)	V_o(V)	I_o(A)	V_o(V)	I_o(A)	V_o(V)	I_o(A)
0.2	5.25	1.50	11.16	3.04	7.77	1.12	6.27	1.71	5.34	1.46
0.4	14.00	3.37	22.70	6.18	15.93	4.33	13.16	3.58	13.17	3.58
0.6	31.50	8.10	34.23	9.31	30.54	8.31	30.60	8.33	30.62	8.33
0.8	84.00	22.11	82.30	22.40	82.55	22.46	82.59	22.47	82.60	22.48

Table 2: Specification of Sepic converter

Parameters	Symbols	Value
Input Voltage	V_{in}	21 V
Output Voltage	V_o	84 V
Switching Frequency	f_s	20 kHz
Resistor Load	R_o	3.675 Ohm
Inductor 1	L_{m1}	122 µH
Inductor 2	L_{m2}	80 µH
Filter inductor	L_f	1 µH
Capacitor 1	C_m	5000 µF
Capacitor 2	C_o	470 µF
Filter Capacitor	C_f	470 µF

Conclusion

This study demonstrates that duty cycle control significantly affects the performance of SEPIC DC–DC converters under resistive loads. Adjusting the duty cycle enables flexible output voltage control, with optimal efficiency and minimized ripple occurring within specific duty cycle ranges. The results reveal that the Sepic dc dc converter is capable of delivering a maximum output power approximately 1857W at dutycycle of 80% with 20 kHz switching frequency. Also, at the same switching frequency, 20% duty cycle, a minimum output power of approximately 5.34 W was obtained. These insights are valuable for power electronics engineers seeking to optimize SEPIC converters for applications with resistive loads, offering a method to enhance converter performance through effective duty cycle management.

Conflict of interest: There is no conflict of interest from the authors.

Acknowledgements: This work was supported by the Department of Electrical and Electronic Engineering, Umudike. The authors wish to thank the staff for their advices and help.

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Citing this Article

Diyoke, G. C., Okeke, C. A., Ezugwu, C., Ozugwu, F. C. & Awah, C. C. (2025). Effect of duty cycle control on performance of Sepic dc–dc buck-boost converter under resistive load applications. *Lafia Journal of Scientific and Industrial Research, 3*(1), 90 – 97. https://doi.org/10.62050/ljsir2025.v3n1.488